Project 4

# Objective

This project is the capstone of Virginia Tech’s Digital Design class within the Computer Engineering department. All skills and techniques from previous projects and assignments culminate in designing a multifunction stopwatch. This stopwatch will be design from project specifications and must be derived from a provided state diagram.

# Design

The design for this project is based entirely off the provided state machine, Figure 1, and a short description of the operation within each state. The basis operation of the stopwatch is a two-function timer that either counts continuously or a countdown function that can be pre-loaded in increments of a millisecond. Based on the project specifications and the state diagram, my implementation used two state machines.

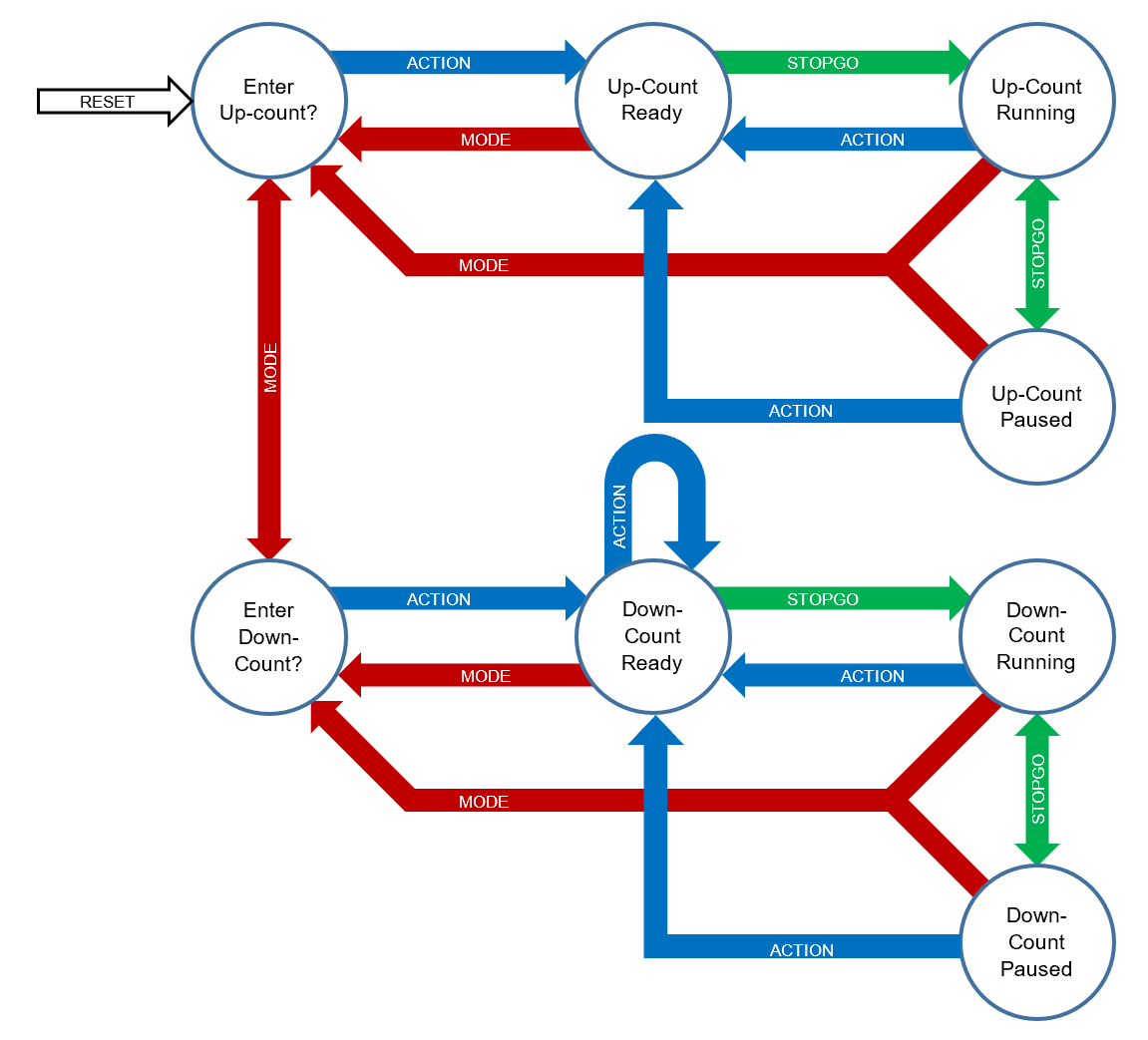


Figure 1. State diagram for stopwatch project

The two machines to operate the stopwatch include one for the controls of the stopwatch and one counter that operates in decimal. The state diagram for the system controller matches exactly to the state diagram provided for operation of the stopwatch. The state diagram for the stopwatch counter matches that provided in HW6. The value outputted was a BCD value for the HEX displays and required six smaller counters internally with the same state diagram .

The control state machine takes in the controls of the DE1-SoC board and handled control of the counter state machine. This design was chosen to allow for each section of the implementation to be clock driven and flow in serial fashion like a Moore machine. The control state machine provided the signals to the counter machine. The counter machine is a decimal counter with six digits to display the time it has recorded. To drive the six digits, six smaller decimal counters were cascaded within the counter machine; one decimal counter’s output controls the input to the decimal counter one magnitude higher. Once the two state machines were designed, thy were simple wired together, pictured in Figure 3.

A screenshot of a cell phone

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Figure 3. Stopwatch block diagram

The above block diagram shows the four layers of this design. The middle two, the two state machines, and the button pressed modules on the left are all clocked elements and lead to full operation that takes a minimum of three clock cycles to execute an instruction. Each button press would move to the control machine, which in turn operated the decimal stopwatch counter. As mentioned above, the stopwatch counter outputted a 24-bit BCD value as inputs to the six seven-segment display drivers.

# Testing

To test the different parts of the system, the modules were tested from the ground up. Starting with the decimal 4-bit counter, the clock divider, then moving to the state machines, and finally to the top-level module of the system. The validity of testing these systems more accurately would be to observe the results after several iterations of the same suite of tests; however, for simplicity several single tests are included below.

## Decimal Counter

The decimal counter was tested in two different ways – testing both the up and down counting functions. This insured that the module could count from 0 to 9 and in reverse, while looping through the values.

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Figure 4. Decimal counter counting up

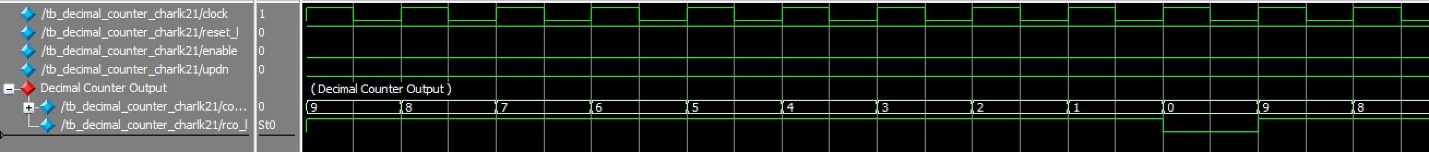


Figure 5. Decimal counter counting down

## Clock Divider

The clock divider was simulated once through to see the frequency that it was active. The circuit was active once for every 50 clock cycles causing the output to be the system clock divided by 50.



Figure 6. Clock divider, 50Mhz to 1MHz

## Stopwatch Counter

Testing the stopwatch counter state machine involved testing if the six individual decimal counters were connected in an accurate way to count up or down in accordance with the decimal counting system without any issues of lagging values. The two figures below show the rollover value and how they affect the value of the counter.

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Figure 7. Stopwatch counter counting up

A close up of a screen

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Figure 8. Stopwatch counter counting down

## System Control

The system control state machine was tested by interacting through its different states achieved by different combinations of inputs. Figure 9 highlights a sample sequence of inouts moving the system through its eight different states and the values of the LEDS that are used to manage the states.

A screen shot of a computer

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Figure 9. System control state transitions

## Top Level Module

The top-level module was the highest module to test. With the assurance that the lower level modules function correctly, the top-level module was tested by operating in its two functions. The two functions are shown below – counting up and a pre-loaded value counting down.

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Figure 10. Stopwatch in continuous up function

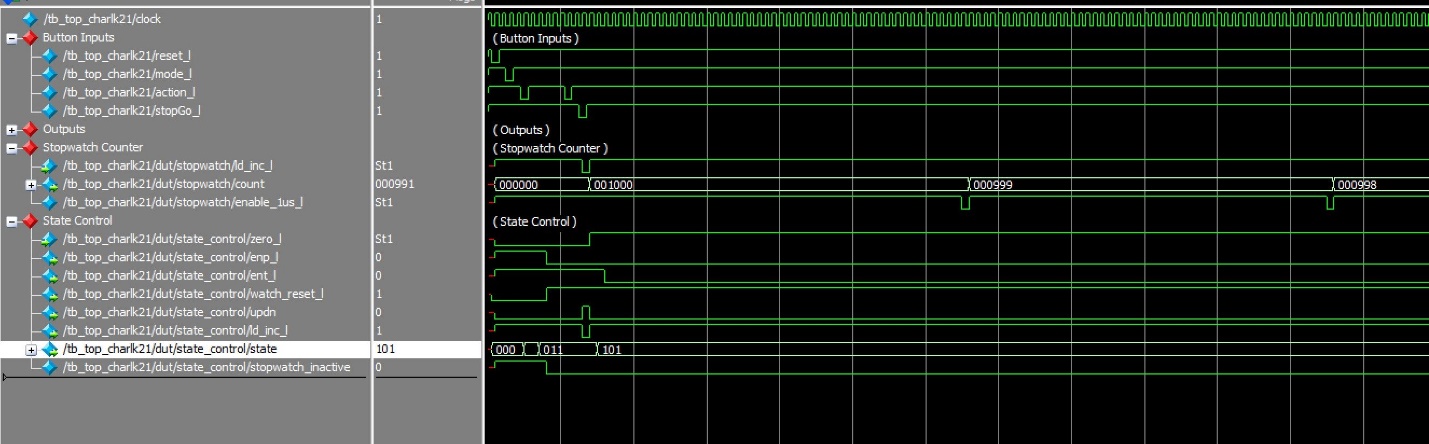


Figure 11. Stopwatch in pre-loaded count down